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(54) Method and System of Ensuring Integrity of Data in an Electronic Memory

(57) Upon recognition that some memory cells in a memory may become defective, the initial data together with the initial address (N_i) are stored at a replacement address (N_i'). A register, further, stores those addresses (N_i) which relate to memory cells or locations which have become defective. When a computer (1) addresses data, a comparator (9) compares the called-for address with the address stored in the defective cell register (10) and, upon equality, routes the data request to the replacement address (N_i') which may be a complete address or a specific location related to a reference address, such as a terminal portion of an auxiliary memory, the main memory, or the like. A warning signal can be given when most, but not yet all, auxiliary memory locations are occupied.

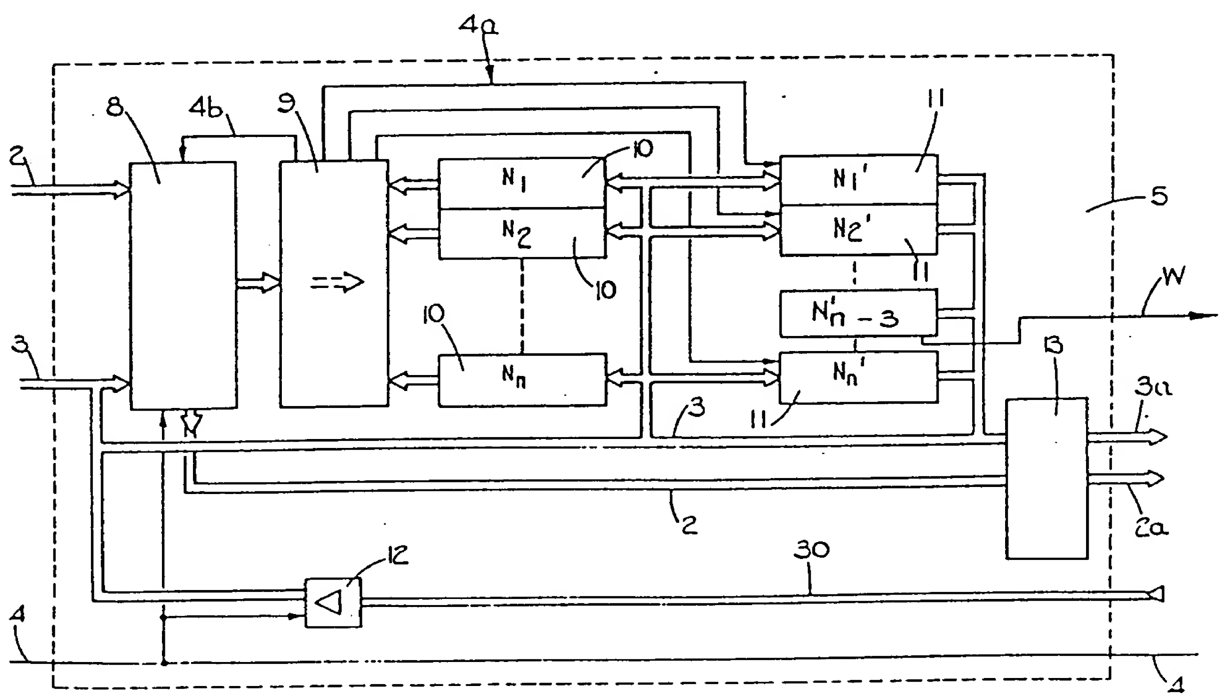

FIG.3.

The drawings originally filed were informal and the print here reproduced is taken from a later filed formal copy.

GB 2 136 992 A

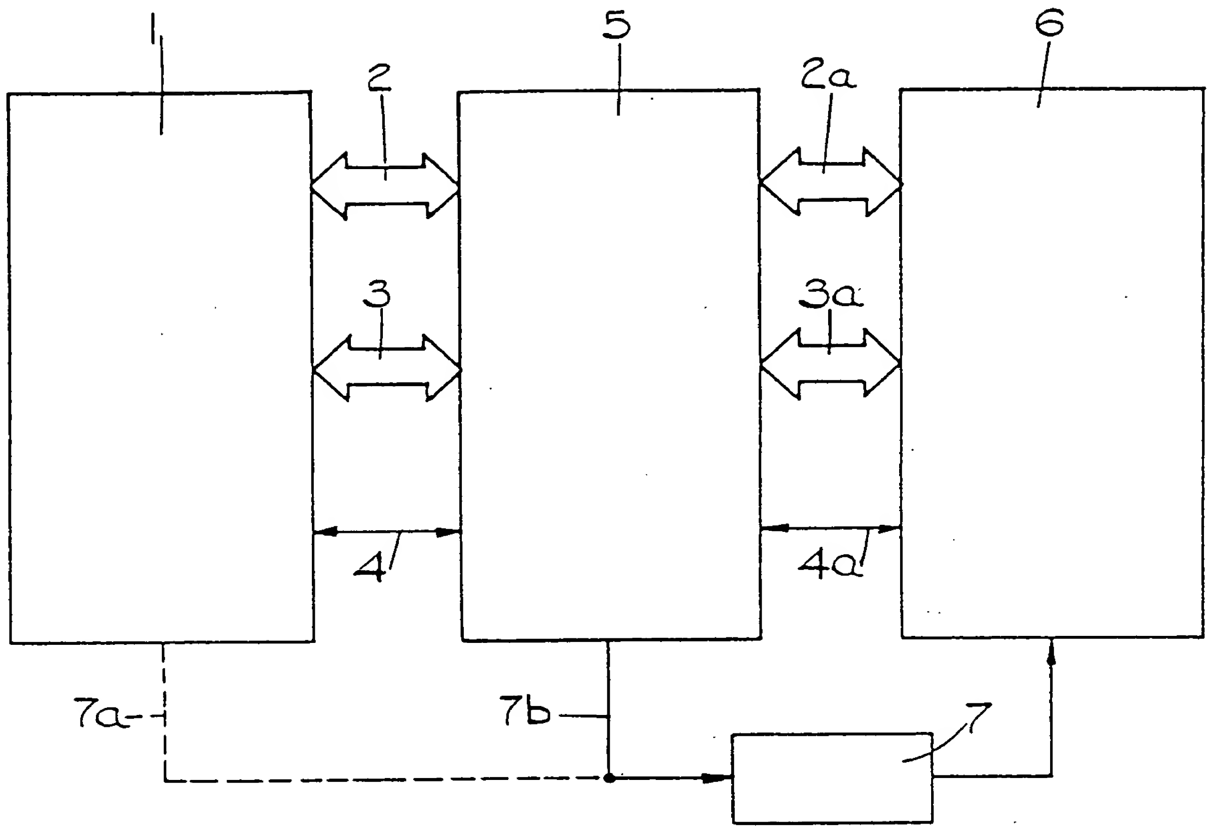

FIG. 1.

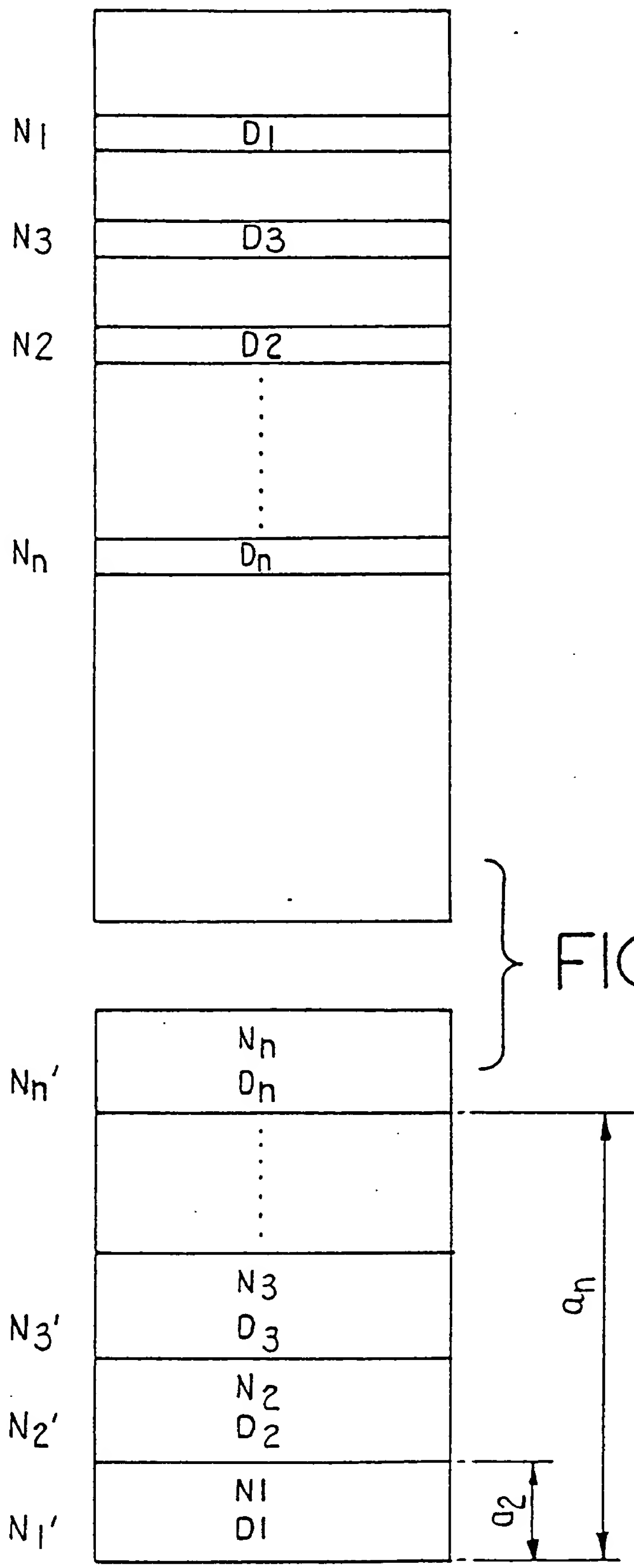

FIG.2.

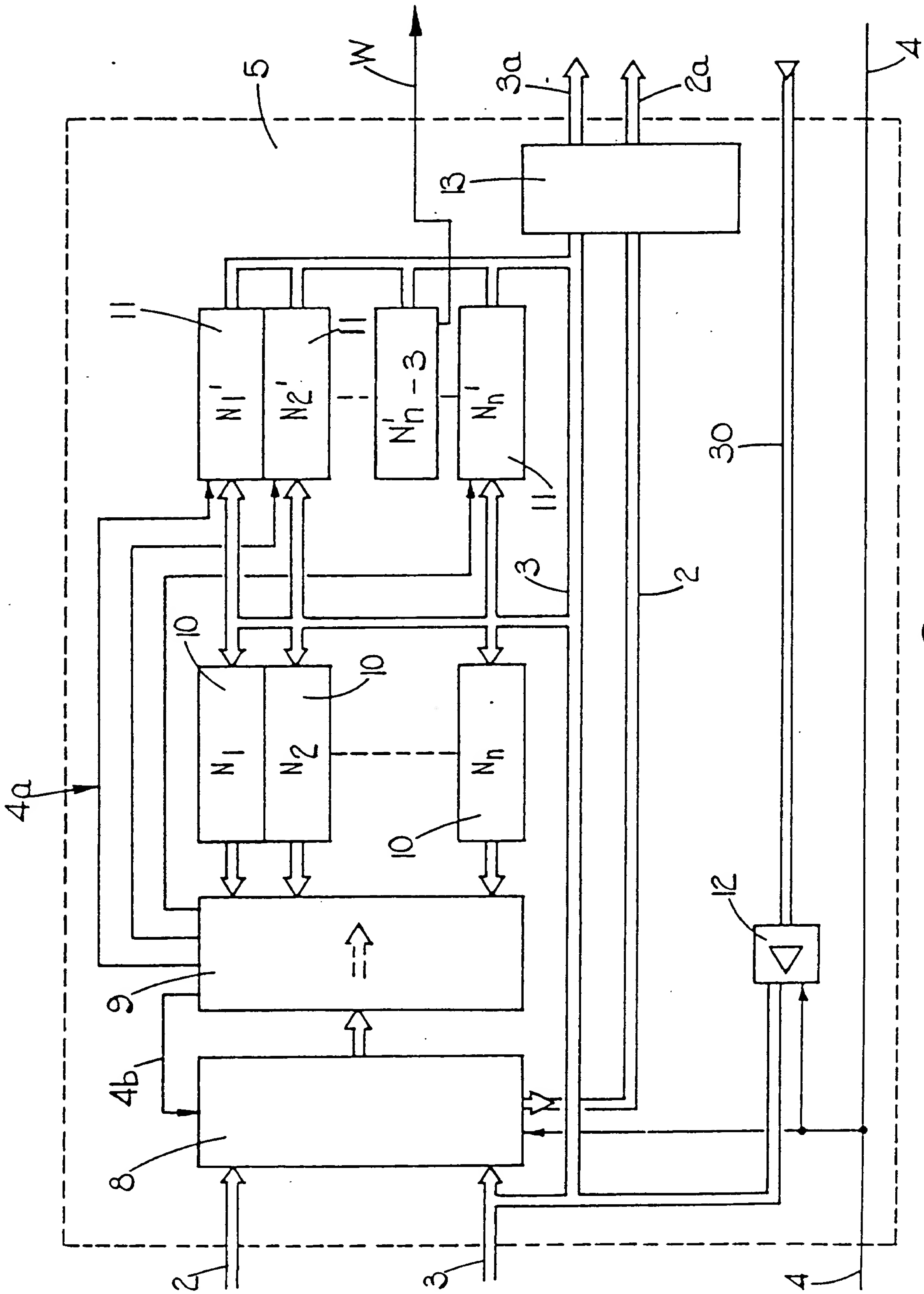

FIG.3.

are compared in a comparator 9 with the initial addresses N_i which are stored in the initial address register 10. The address register 10, forming the original address memory, stores only those addresses which relate to defective memory cells, or to cells which tend to become defective, as determined for example in accordance with the disclosure of the German Offenlegungsschrift DE—OS 28 53 925. If no comparison is indicated by comparator 9, that is, if the address supplied by address bus 3 does not have an equal address of a defective cell, the address line 3 is directly connected from the input register to the output register 13 for subsequent connection to the commanded address in the memory 6 on the output address line 3*a*. If, however, a correlation is established between an address in the register 10 and the address on bus 3 derived from processor 1, the address in the input 8 is blocked and, rather, a corresponding replacement address N_i', stored in a register forming the replacement address memory 11, is connected to the output register 13. Control of the respective comparison, and either through switching of the address from bus 3, or switching of the replacement address from memory 11 is effected by control connecting lines 4*a*, 4*b*, which interconnect the register positions of the replacement address memory 11, the address comparator 9, and the input register 8. The data which are stored either in good cells forming the original address or in cells at the replacement address are read-out over a return data bus 30 through a buffer 12 and the data bus 3. Other read-out arrangements, for example connecting of the buffer 12 to the data bus 2, of course, can be used, in dependence on the system's concept. Control and timing are effected by suitable signals on the control bus 4.

The replacement address memory 11 may store either a complete address or an address with respect to a reference address. Storing data with respect to a reference requires, usually, a lesser number of addressing bits than storing a complete address. It requires, however, a computation section which reconstitutes a complete replacement address which includes the reference address as well as the particular location from the reference address.

A further possibility is this: The address register 11 may receive the data D_i directly, and in such arrangement, storing and providing a replacement address N_i' in the memory correction unit can be entirely eliminated. Upon placing the initial address N_i in the memory correction unit, then, the additional information D_i must also be placed therein. This provides for a very compact storage of replacement addresses, provided, however, the bits required for the data, that is, the set of data bits, is no longer than the address itself.

The system and method permits correction of data, as well as prevents loss of data. There is no overprogramming. It avoids the necessity of continuously and prophelactically refreshing memories which, as known, degrade upon continuous re-programming. Thus, inherently perfectly operating memory structures may be abused by continuous re-programming. Such abuse is avoided by only selecting for exchange of addresses those cells in which a trend towards defective operation has been discovered. The requirement for redundancy in storage of memory locations is substantially reduced since, from experience, only a small portion of memory cells in an overall memory may become defective.

A warning signal can be generated, for example, by a replacement address memory 11 when all but three of the replacement addresses are occupied, as schematically shown by the fragmentary address memory N_{n-3}', providing a warning signal over line W that only two more replacement memory locations are available.

CLAIMS

1. Method of ensuring the integrity of data in an electronic memory particularly including erasable programmable read-only memory elements (EPROMs) forming said memory unit, in case of incipient or actual malfunction of one or more data storage cells in the memory unit, in which the data are stored at auxiliary memory locations, comprising storing the original data together with the original address in the auxiliary memory cell or replacement memory location at a replacement address.

2. Method as claimed in claim 1, including the step of storing replacement addresses in a correction or replacement address memory.

3. Method as claimed in claim 2, including the step of storing the replacement addresses in a correction or replacement address memory section forming a portion of said memory unit.

4. Method as claimed in claim 1, including the step of generating a replacement address inherently characterising the replacement address of the auxiliary memory cell.

5. Method as claimed in claim 1, including the step of generating a replacement address with respect to a reference address or reference location of a replacement address memory unit.

6. Method as claimed in claim 5, in which said reference address is a terminal address of said correction memory unit.

7. Method of ensuring the integrity of data in an electronic memory particularly including erasable programmable read-only memory elements forming said memory unit, in case of incipient or actual malfunction of one or more data storage cells in the memory unit, in which the data are stored at auxiliary memory locations comprising the steps of re-storing the original data stored at an original address in an auxiliary memory at a replacement address together with the original address, addressing the original address, and determining if the original address contained data subject to malfunction of the memory and, if so, retrieving said data with reference to the original address in the auxiliary memory location.

8. Method as claimed in claim 1 or 7, including

SPECIFICATION

Method and System of Ensuring Integrity of Data in an Electronic Memory

The present invention relates to a method and system of ensuring integrity of data in an electronic memory and more particularly to electronic memory elements or units which are installed on-board an automotive vehicle to store information and data relating to the operating characteristics of the vehicle engine for example data relating to ignition timing and the like.

Various types of memory units which include memory elements or cells use erasable programmable read-only memories (EPROMs). Such memory elements or cells may be formed by two serially connected field effect transistors (FETs), in which one FET acts as a constant current source, and the other changes its resistance under control of pulses applied to the gate thereof. Read-out of the stored data, which are represented by either high or low resistance values of the controlled FET, and hence the voltage thereacross, is obtained by determining the voltage level at the junction between the main current carrying paths of the two serially connected FETs.

It is known that memory cells of this type can change their data storage characteristics due to various external influences which particularly include temperature, incidence of light, penetration of moisture or humity, and the like. German Offenlegungschrift DE—OS 28 53 925 described such changes. Change in the characteristics of operation of the EPROM may be caused by external effects which detract from the insulating capability of the gate of the FET, so that charge carriers may leak off from the gate. The opposite effect may, however, occur, namely that charge carriers can be applied to the gate of a storage cell, for example because insulation to the surrounding area is defective, or energy is being applied thereto, for example by leakage of light. The change in charge state of the gate electrode usually is not abrupt, but rather is a gradual, slow change; yet after some time, the charge will be lost.

It has previously been proposed to avoid loss of charge on an EPROM by refreshing the date stored therein. The on-board control computer for a motor vehicle, for example, can be so arranged that a refreshing circuit reprograms the EPROMs of the memory at uniform intervals. This method can be used, however, only if the memory cells are still at least of such integrity that their original data can be read out, for reprogramming or refreshing the date therein. Refreshing the data in a memory cell of course will not lead to the desired result if the cell itself is defective, and the loss of the data is not caused by external influences.

Loss of data in a memory can be avoided by providing redundant storage. It is, for example, possible to store all data twice in a memory of sufficiently large storage capacity and then provide comparisons or subtractions or summing of the data stored in the respective memories, and then, with a test program, determining which set of data in the two memories is in order, and which may have been stored in a defective manner. The requirement of memory capacity in such units is, however, high, which substantially increases the price of the electronic equipment, contributes to complexity, which is another cause of possible malfunction, and requires additional space and auxiliary equipment.

It is an object to provide a method and system in which the integrity of data stored in electronic memories, particularly in EPROMs of the multiple field effect transistor (FET) type, can be ensured, so that the data will always be available, correctly, for processing in a computer, and especially in an on-board computer of an automative vehicle.

Briefly, it is suspected that a specific data cell has a tendency to become defective, the original data, together with the original address, are stored in an auxiliary memory cell, or a replacement memory which may have only a substantially smaller number of memory addresses and locations than the overall memory itself, together with a replacement address.

In accordance with a feature of the invention, the original address is addressed by the compute and a determination is made if the original address stores data subject to malfunction of the memory; if so, the data are then addressed with reference to the original address in an auxiliary memory location.

In accordance with a feature of the invention, memory correction unit is provided, located between the computer and a memory unit, the memory correction unit including a comparator i which addresses which are supplied by the computer are compared with the addresses stored therein, the addresses stored in the memory correction unit, of course, being those which relate to defective memory cells. If the comparator indicates equality—in other words, that an addressed memory location is in a defective storage cell—a replacement or auxiliar address then will be addressed.

The method and system has the advantage that only the data on those addresses which characterize data cells which are or may become defective need be stored in a replacement or auxiliary address, together with the original address. Usually, only a few memory cells of a memory unit will be defective; thus, it is only necessary to provide only so many replacement auxiliary cells at respective replacement or auxiliary addresses which, reasonably, may be required to replace possibly defective cells or ce which become defective in course of time. Consequently, only a comparatively small numb of additional memory cells are required in order ensure operating reliability and storage of the required data and programs for a computer, and especially for an on-board vehicular type computer.

the step of providing a warning signal if a predetermined number of replacement addresses have been occupied by data.

9. System to ensure the integrity of data in an electronic memory unit particularly including erasable programmable read-only memory elements (EPROMs) in case of incipient or actual malfunction of a data storage cell in the memory and having a computer connected to the electronic memory unit, and comprising a memory correction unit connected between the computer and the memory unit and including a comparator means for storing addresses of memory cells or memory locations which are subject to possible malfunction connected to the comparator; and a replacement address memory storing replacement addresses, said comparator comparing an address supplied thereto from the computer with the address in the possible malfunction address storage means, the comparator providing an output signal upon equality to supply data to the computer from a replacement address as determined by the replacement address memory.

10. System as claimed in claim 9, in which said memory correction unit comprises an input register and an output register for temporary storage of addresses or data.

11. System as claimed in claim 9, in which the means for storing addresses of possible malfunctiong memory cells or locations comprises a first register and in which the replacement address memory comprises a second register in the form of a complete address.

12. System as claimed in claim 9, in which the means for storing addresses of possible malfunctioning memory cells or locations comprises a first register and the replacement address memory comprises a second register storing the distance of replacement addresses from a reference position or reference address.

13. System as claimed in claim 9, in which the means for storing addresses of possible malfunctioning memory cells or locations comprises a first register and the replacement address memory has sufficient memory locations for storing the original address and the data at a replacement address location.

14. System as claimed in claim 9, in which the means for storing addresses of possible malfunctioning memory cells or locations comprises a first register and the replacement address memory has sufficient memory locations for storing the original address and the data at adjacent replacement address locations.

15. System as claimed in claim 9, in which said comparator is connected to an input register and said replacement address memory is connected to an output register to respectively control one of said registers to change the address data as received to modified output address data in the output register for addressing of data in replacement addresses.

16. Method of ensuring the integrity of data in an electronic memory substantially as herein described with reference to and as illustrated in the accompanying drawings.

17. System to ensure the integrity of data in an electronic memory unit substantially as herein described with reference to and as illustrated in the accompanying drawings.

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